Power Efficient Current-Mode SAR ADC for Memristor Readout in 28 nm CMOS

Anugerah Firdauzi*, Christian Grewing*, Arun Ashok*, Sabitha Kusuma*,
Kay Winterberg*, André Zambanini*, and Stefan van Waasen*†
*Central Institute of Engineering, Electronics and Analytics – Electronic Systems (ZEA-2)
Forschungszentrum Jülich GmbH, 52428 Jülich, Germany
†Faculty of Engineering, Communication Systems, University of Duisburg-Essen, 47057 Duisburg, Germany
E-mail: a.firdauzi@fz-juelich.de

***Abstract*—This paper introduces a current-mode Successive-Approximation Register Analog-to-Digital Converter (SAR ADC) for the current readout in a memristor based vector-matrix multiplication for computing-in-memory. The proposed method employs direct current measurement scheme using an open-loop transimpedance input stage. As the types and resistance values of the memristors change, so does the output current of the array, along with the voltage range, especially with multilevel signal processing. Therefore, we propose an ADC where the dynamic range can be tuned between 0.4 and $1.28\,\mathrm{mA}$ while consuming 1 to $2.73\,\mathrm{mW}$ of power. While the memristor array operate at a $1.8\,\mathrm{V}$ power supply for SET and RESET operation, the ADC can be implemented using a $0.9\,\mathrm{V}$ power supply as we employs a voltage-regulation loop that can work with less than $0.8\,\mathrm{V}$ voltage during current readout mode. This enables the ADC to be implemented using core CMOS devices, reducing power and area consumption. The ADC features $6\,\mathrm{bit}$ resolution and is implemented in a $28\,\mathrm{nm}$ CMOS bulk technology. It can achieve a data-conversion rate of up to $50\,\mathrm{MSps}$.**

***Index Terms*—SAR ADC, current measurement, memristor, Vector-Matrix Multiplication, Computing-in-Memory**

I. Introduction

Computing-in-Memory (CIM) is a promising method to address the bottleneck inherent to traditional von Neumann computing architectures. As depicted in Fig. 1, one potential implementation involves utilizing memristor based crossbar arrays, which store information as resistance or transconductance, enabling highly parallel Vector-Matrix Multiplication (VMM) [1]. In this configuration, Digital-to-Analog Converters (DACs) deliver input voltages to the crossbar rows, the resulting output currents are summarized for each column and subsequently measured by Analog-to-Digital Converters (ADCs). Hence, both converter circuits play pivotal roles in optimizing operational speed and power consumption.

In [2], a charge integration method was used to measure the current generated by the memristors. As illustrated in Fig. 2, current is first sampled by a switch and integrated on a capacitor over aperiod of time. For this kind of approach, a switched-capacitor (SC) integrator is often employed to allow measurement of very small input current from multiple sources at a different time. In [3], a $\Delta\Sigma$ structure was employed to improve data-conversion resolution while needing a longer time for the conversion.

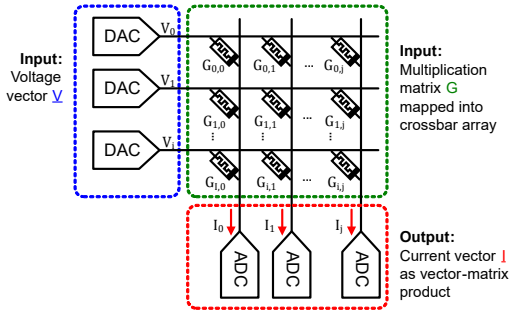

Fig. 1. Memristor-based crossbar array using transconductances to enable highly parallel Vector-Matrix Multiplication.

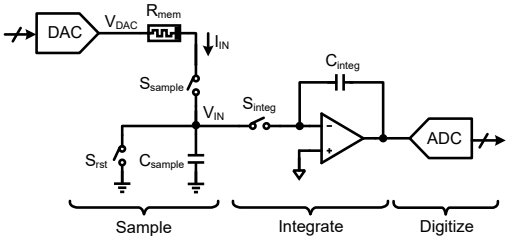

Fig. 2. Charge-integration method for current measurement [2].

While an SC integrator seems to use, depending on the capacitance value, a small area and low power consumption, the op-amp will be the dominant circuit with respect to area and power consumption. Additionally, as the memristor is not actually a current source, the current flowing is also depends on the sampled voltage at the capacitor. Moreover, the dynamic range and speed of the ADC greatly depends on the pulse width of the signal used for sampling, where a clean reference clock would be required. Furthermore, the range of detectable current values depends on the capacitance and the available headroom.

In this paper, we propose a direct current-measurement method illustrated in Fig. 3(a) which utilizes a current-mode Successive-Approximation Register (CM-SAR) ADC. In this structure, the memristor is integrated into a voltage-regulation loop to maintain a stable voltage (and consequently current) during measurement. This ADC is also designed in a way that

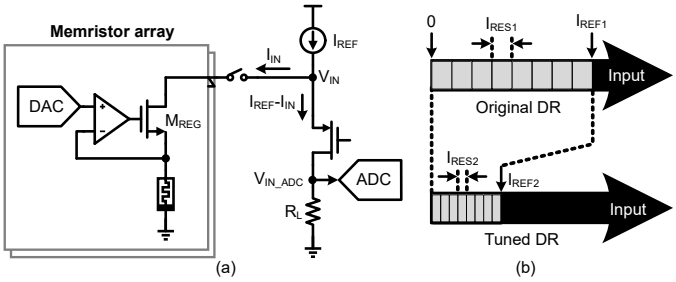

Fig. 3. (a) Proposed current-measurement. (b) Proposed dynamic-range tuning method.

its dynamic range (and thus also its resolution) can be easily adjusted depending on the system requirements by changing the value of the reference current as depicted in Fig. 3(b). This method will allow the ADC to achieve a finer precision and adapt its power consumption to the actual requirements.

II. Proposed ADC Architecture

A. ADC Bias

The detailed architecture of the proposed current-mode SAR ADC is shown in Fig. 4. For the ADC bias, we propose a low-headroom cascode circuit using transistor M_{0-3}. The voltage of V_{BP0} is formed from the diode connection of $M_{0,1}$. As for V_{BP1}, a series resistance is often employed to provide a voltage difference of $V_{\mathrm{BP0}} - V_{\mathrm{BP1}}$ [4]. This method, however, is prone to process, voltage, and temperature (PVT) variation that may cause the transistors to operate outside saturation region. Moreovoer, this method is also not suitable for this work as the reference current, I_{REF}, will be adjusted all the time depending on our measurement range. For this reason, we are using NMOS $M_{2,3}$ to reduce the headroom of the transistors M_0 and M_1.

The bias voltages generated by these cascoded PMOS are then used to bias the output stage of the ADC (M_{6-10}) and the current steering DAC of the SAR. Additionally, it also sets the dynamic range of the ADC to be equal to the value of I_{REF}. Furthermore, by simply changing I_{REF}, the dynamic range of the ADC can be tuned depending on the system requirement. In this implementation a large reference current is used to ensure robustness against coupling from the switching of the ADC. Since the bias will be shared for several ADCs to reduce area and power consumption, a reduced current and a buffering of the reference voltages will be preferred.

B. ADC Core Circuit

While this ADC is a single-ended one, a differential implementation of the DAC is chosen to make the circuit less prone to noise and coupling. The pair of cascoded PMOS current sources $M_{7,8}$ and $M_{9,10}$ deliver each $0.5I_{\mathrm{REF}}$ of current to ensure that the circuit stays within a linear operation point. At node V_{IN}, the input current from the memristor based tile is drawn from the the current of the source implemented by M_6. Thus, the current through M_8 will change accordingly. The current difference of the two cascode transistors $M_{8,10}$ will cause a voltage difference across the variable load resistances R_{L}. For a measurement up to $1.28\,\mathrm{mA}$, R_{L} is set to $350\,\Omega$ to make the voltage swing between 0 to $450\,\mathrm{mV}$. The resistance range can be programmed to ensure that the input voltage to the comparator is sufficient.

Data conversion is then performed using SAR algorithm with an array of current-steering DAC. For an N-bit ADC, only an N-1 bit DAC is required as the input subtraction with half of the reference current can be considered as the MSB conversion. While the DAC is pulling a current from one branch it will reduce that amount of current from the opposite branch, resulting in a double current change. Consequently, for this structure, an LSB current of $I_{\mathrm{REF}}/2^{N+1}$ is required for the current-mode cell. In this structure, the sum of the current flowing through M_7 and M_9 needs to be equal the maximum current pulled by the steering DAC, which is also equal to half of the dynamic range of the ADC. Additionally, the amount of current flowing through M_6 and M_7 will determine how much current can actually be measured by the ADC. When the input current is low, a current of $0.5I_{\mathrm{REF}}$ at $M_{7,9}$ is sufficient. However, when the input current is close to I_{REF}, an offset up to $0.25I_{\mathrm{REF}}$ may need to be added to $M_{7,9}$ to keep all the transistors working in the saturation region. With this, the current consumption of the ADC can be set with in a minimum range depending on the actual requirements of the array.

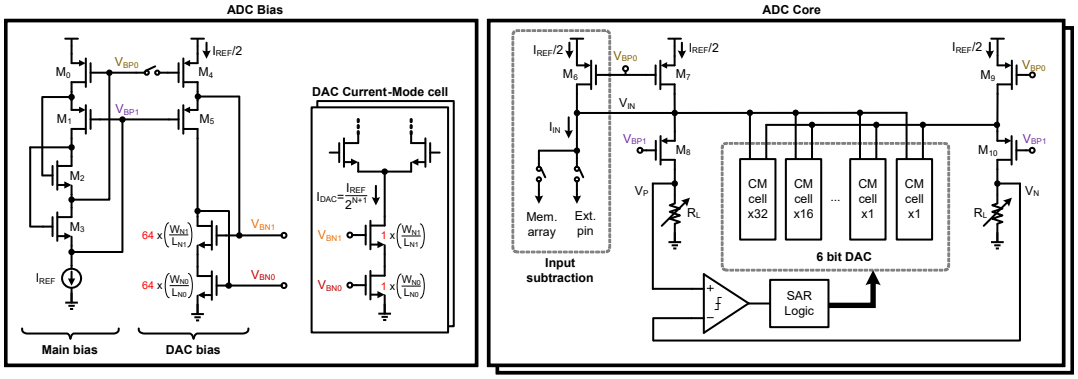

Fig. 4. Architecture of the proposed 6 bit Current-Mode SAR ADC.

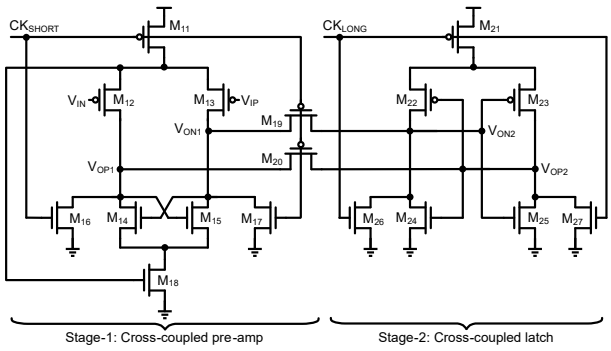

Fig. 5. Dynamic comparator circuit.

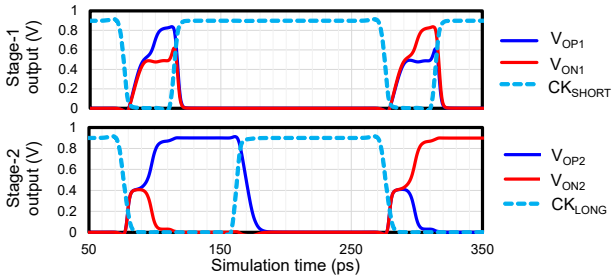

Fig. 6. Dynamic comparator simulation.

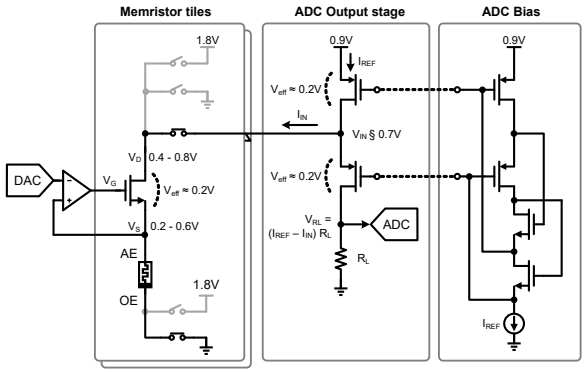

Fig. 7. The interface between the ADC and the memristor.

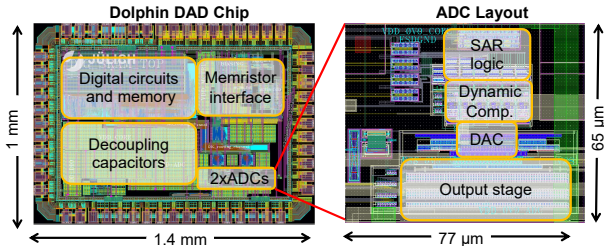

Fig. 8. Layout of the chip and the ADC

C. Dynamic Comparator

The structure of the dynamic comparator is shown in Fig. 5. As shown in the simulation results of Fig. 6, at initial state, both CK_{SHORT} and CK_{LONG} signals are at high voltage to reset the value of V_{O1} and V_{O2} to ground using $M_{16,17,26,27}$. Next, CK_{SHORT} is at low voltage which will allow $M_{12,13}$ to perform voltage amplification and the latch on $M_{14,15}$ will add amplification to the voltage difference of V_{ON1} and V_{OP1}. The current difference generated by the pre-amp is then picked up by the cross-coupled latch in the second-stage (M_{22-25}). When signal CK_{LONG} is set to low voltage, this current difference will set the output voltage of V_{O2} to CMOS values. Signal CK_{SHORT} is then turned off after output is latched to avoid any static current flowing from $M_{12,13}$ to sinking into transistor $M_{14,15,24,25}$.

This pre-amp structure is similar to the strong arm latch [5], but the proposed comparator has more dynamic range as it has less transistors stacked between the V_{DD} and the ground. This structure is also similar to the double-tailed latch in [6], but the proposed structure is faster and more sensitive thanks to the use of cross-coupled latch at the pre-amp stage.

D. ADC and Memristor Interface

In this research project, the ADC will be used with the memristor model JART VCM v1b developed for HfO_2/TiO_x-based ReRAM Cell [7]. In this model, a voltage of $1.5\,V$ is required to reset the memristor and bring it from low-resistance state (LRS) into high-resistance state (HRS). For this reason, most of the circuits to control the memristor are implemented using I/O CMOS device that works at $1.8\,V$ power supply. As shown in Fig. 7, during memristor readout mode, pin OE is connected to the ground while pin AE is connected to voltage-regulatied node controlled by the DAC, with value ranging from 0.2 to $0.6\,V$. The NMOS regulator is designed to work at effective voltage, $V_{eff} = V_{GS} - V_t = 0.2\,V$, and thus a minimum V_D voltage of 0.4 to $0.8\,V$ is sufficient to keep the NMOS working at saturation region. At the ADC output stage, node V_{IN} is connected to node V_D through a transmission gate designed using I/O CMOS devices with power supply of $1.8\,V$ isolating the ADC from the memristor outside of readout mode. The value of node V_{IN} is set by the cascode transistor $M_{0,1}$ at the ADC bias circuit shown in Fig. 4, which is around $0.7\,V$, and thus still within the required voltage range of V_D. Therefore, while the memristor tiles are implemented using $1.8\,V$ I/O CMOS devices, it is possible to implement the ADC using the smaller and faster core CMOS devices with $0.9\,V$ power supply.

III. ADC Implementation and Simulation Results

This ADC is implemented using $28\,nm$ CMOS, and its layout is depicted in Fig. 8, showing a less than $0.005\,mm^2$ area. While this area is small enough for the ADC to be used multiple times, for future work, a rectangular size with smaller height (or length) less than $20\,\mu m$ is preferred so more ADC can be used in the same column (or row). In this work, six dynamic comparators are used to speed up the ADC by reducing the wiring between the DAC and the SAR logic. However, in this very small footprint of the ADC, the parasitic capactors of a central sequencer are not significant. For future work on this ADC, using just a single comparator is preferred to achieve a smaller area.

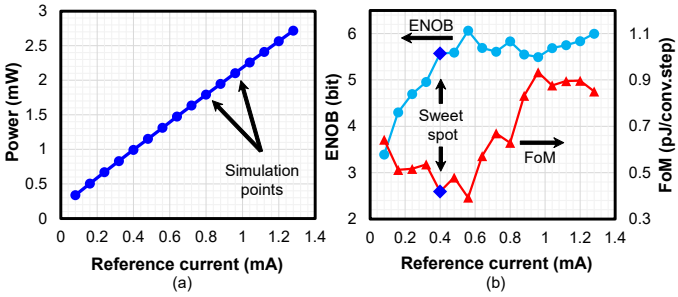

Fig. 9. ADC simulation with reference current sweep. (a) Power consumption. (b) ENOB and FoM

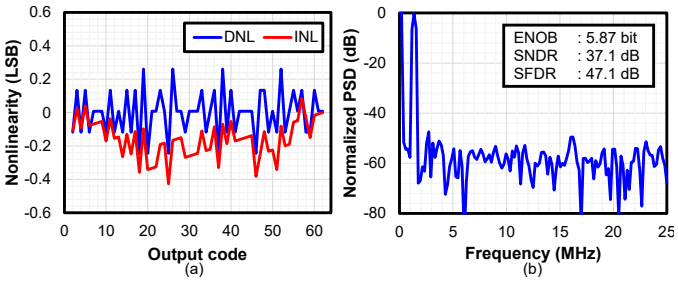

Fig. 10. (a) Static performance of the ADC and (b) the spectrum of the ADC.

The post-layout simulations show that the ADC can run at a maximum conversion speed of 50 MSps. To check the range of the tunability, the reference current is swept from 80 µA to 1.28 mA, and as depicted in Fig. 9(a), its power consumption is proven to be proportional to the reference current. From this graph, it can also be extrapolated that the digital circuit consumes 197 µW power consumption regardless of the reference. Note that the bias circuit is omitted from power consumption calculation as only one central bias will be required for several ADCs of one array.

When the reference is reduced from 1.28 to 0.4 mA, the effective number of bits (ENOB) is stable around 5.5 bit and the Figure of Merit (FoM) also keep decreasing following the reduction in power consumption, as depicted in Fig. 9(b). When the reference current is lower than 400 µA, there is a sharp decrease of ENOB and sharp increase of FoM as the transistors can no longer work in saturation region.

The simulation results with a 1.28 mA reference are shown in Fig. 10. A static simulation using a ramp input signal reveals a differential nonlinearity (DNL) less than 0.3 LSB and integral nonlinearity (INL) of less than 0.45 LSB. Additionally, a dynamic simulation with a 2.54 kHz sinusoid input demonstrates an ENOB of 5.87 bit.

While many papers discuss ADCs for CIM, they often lack details about individual performance. Therefore, we compare the proposed CM-SAR ADC with ADCs used for biological sensors. Table I shows the performance comparison. Although this ADC has a lower SNDR than other architectures, it excels in speed and has a comparable figure of merit. Compared to the counter-based ADC in [8], which also has a wide measurement range, our ADC demonstrates superior speed due to the direct current-measurement method. Note that the power consumption of this ADC accounts for the measured current, resulting in higher power consumption relative to its dynamic range.

TABLE I
PERFORMANCE COMPARISON OF ADCS FOR CURRENT MEASUREMENT.

Parameter	[8]	[9]	[10]	This[a]	
Architecture	Coarse-fine cntr	ΔΣ counter	Slope counter	CM-SAR	
CMOS (nm)	180	180	180	28	
V_{DD} (V)	1.8	1.8	1.8	0.9	
F_S (Sps)	2.5k	100k	2k	50M	
F_{BW}(Hz)	1.25k	18	1k	25M	
Max range (µA)	512	10	200	400	1.28k
SNDR (dB)	96.12	140	119	35	37.1
ENOB (bit)	15.7	23	19.5	5.5	5.87
Power (µW)	79.4	295	196	1k	2.73k
FoM (pJ/conv.)[b]	0.61	1	0.13	0.44	0.93

[a] Based on post-layout simulation results
[b] FoM = Power/(2 × F_{BW} × 2^{ENOB})

IV. CONCLUSION

A 6-bit current-mode SAR ADC in 28 nm CMOS is proposed for memristor readout in CIM applications. By employing a direct current-measurement method, the measurement range can be easily adjusted by simply modifying the reference current to reduce the power consumption significantly. It is designed with reference between 400 µA to 1.28 mA in mind. Notably, no op-amp, TIA, or S/H circuit is necessary for this ADC, resulting in power and area savings and a large input current range.

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